Design and Characterization of a 0.9-V Differential Inverter-Based OTA

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***Abstract*—Operational transconductance amplifiers (OTAs) are important building blocks for many electronic circuits such as analog filters and data converters. Sub-1V analog circuits are becoming popular for Internet-of-Thins (IoT) applications due to low power consumption. In addition, digitally based OTAs have been explored with the aim of achieving high energy efficiency. This paper involves the implementation of an inverter-based OTA with self-biasing technique to operate in the common-mode band through the implementation of a differential difference amplifier in order to mitigate unwanted variations operating in weak inversion. The OTA is designed on 180-nm CMOS technology and powered by a 0.9-V power supply. A DC gain of 52.22 dB was achieved with GBW close to 36.66 MHz. Power consumption was 203.71 μW for a load capacitance of 10 pF.**

***Index Terms*—OTA inverter, differential amplifier, self polarization, low voltage.**

I. Introduction

In the current scenario, there is an increasing adoption of wearable technologies and smart devices with diverse circuit capabilities. Most electronic devices related to consumer electronics are battery powered, thus the energy consumption reduction is a key goal in current electronic circuits design. However, there are challenges in the design of electronic circuits, such as to keep the performance of analog circuits within successively reduction of supply voltages.

The operational transconductance amplifier (OTA) is an important building block for the development of electronic circuits since it is widely used in active filters and analog-to-digital converters [1]–[4]. It is also usually used to active-RC integrators or Gm/C integrators.

In the last years, different low-voltage OTA topologies have been introduced in the literature for applications with supply voltage ranging from 0.3-0.5 V [5]–[7]. However, the supply voltage reduction is limited by the minimum threshold voltage of the transistors, and also by the signal-to-noise ratio (SNR) required by the application.

Lately, traditional OTA topologies based on gate-driven differential pair have been replaced by bulk-driven differential pair OTAs or even OTAs based on logic gates.

Inverter-based amplifiers have several features for integrated circuit design, as they have higher transconductance efficiency compared to conventional OTAs. In this way, the CMOS transistors used in these circuits operate with low supply voltage and low power consumption [8].

A recurring problem of inverter-based OTAs is their unstable common-mode voltage. Several strategies are used to make the circuit more robust to these oscillations. Common-mode voltage control by the bulk terminal of transistors is the most used strategy. However, some CMOS technologies cannot isolate the bulk region of NMOS transistors. One strategy is the use of current sources to bias the OTA transistors. Thus, their currents are dependent on the common-mode feedback.

This work presents the design and analysis of a 0.9 V inverter-based OTA in a 180 nm CMOS process for use in low-power data converters. The common-mode control is performed through current sources dependent on common-mode feedback. The common-mode feedback circuit is implemented with a a differential difference amplifier (DDA) to correct unwanted voltage fluctuations without influencing the performance of the main amplifier.

The remaining of this paper is organized as follows: Section II presents OTA topology; Section III presents the schematic-level simulation results; and concluding remarks are given in Section IV.

II. OTA Inverter Implementation

The OTA topology which is designed and analysed in this work is presented in Fig. 1. This circuit is a simplified version of the original one that was initially introduced in [9]. It is an inverter-based OTA with two control transistors. This OTA was designed with a reduced supply voltage of 0.9 V in a 180-nm CMOS technology.

The CMOS inverters are composed of transistors M1-M2 and in M3-M4. The input signals are applied at the inverters input and the OTA output is at the inverters output. Transistors M5-M6 serve to control the output common-mode voltage level. The control voltage Vctrl is generated by the common-mode feedback circuit (CMFB). Since PMOS and NMOS transistors have a bulk connected directly to VDD and ground, respectively, it is evaluated that M5 and M6, together with the OpAmp of Fig. 2, adjust the DC gain of the OTA inverter to resist to adverse oscillations. The Vctrl signal is refined to keep the OTA operating in the desired $\frac{VDD}{2}$ region also for the common mode voltage (Vcm).

The DC gain of the designed OTA is given by:

$$Av = \frac{gm_1 + gm_2}{gds_1 + gds_2} \tag{1}$$

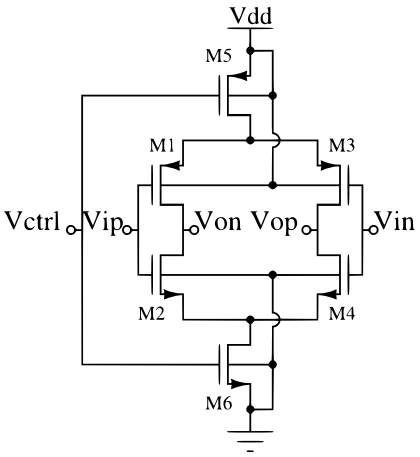

Fig. 1: Schematics of the designed inverter-based OTA.

Standard-V_T transistors with a threshold voltage of $\sim 500\ mV$ are used in the design. Thus, the CMOS inverter transistors work in weak inversion, providing a high-transconductance efficiency. With this, it is possible to achieve a DC gain higher than 40 dB at cost of increasing silicon area.

A. Common Mode Feedback Circuit (CMFB)

Fully-differential amplifiers require a common-mode feedback circuit to ensure the common-mode output voltage stability. This is achieved by sensing and comparing the common-mode output voltage with a voltage reference, and then generating a control signal to the main amplifier.

With the self-biasing technique explored in [10], a differential amplifier is introduced to establish the Vctrl value in order to support PVT variations and reduce the need for regulators that would hinder the circuit accuracy.

Figure 2 presents the configuration of the designed DDA for application in the inverter-based OTA, which has as input a common mode voltage (Vcm) that forces a control voltage (Vctrl) to $VDD/2$.

The circuit compares the OTA output signals Von and Vop with the common mode voltage Vcm and generates an error signal Vctrl which is feedback to the OTA, thus keeping the circuit stable to variations.

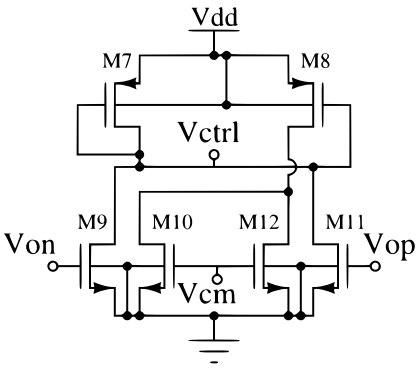

Fig. 2: Topology of the implemented Differential Difference Amplifier (DDA).

TABLE I: Dimensioned OTA transistors sizes.

Transistor	Type	W (μm)	L (μm)	Multipliers
M1, M3, M5	PMOS standard	15.7	1.0	70.0
M2, M4, M6	NMOS standard	2.0	1.0	70.0
M7, M8	PMOS standard	14.0	1.0	70.0
M9-M12	NMOS standard	2.0	1.0	70.0

B. Design Optimization

The circuit was initially analyzed so that the output signal was set to $\frac{VDD}{2}$. The channel length of the transistors was fixed in 1 μm and channel width for all NMOS transistors was kept fixed in 2 μm in both OTA and CMFB circuits. However, the width of PMOS transistors were varied so that the output signal could operated in the desired range, with the number of multipliers (fingers) set to 70 for all transistors.

Therefore, a separate analysis was performed for the OTA with Vctrl connected to a voltage controlled voltage source. The first control signal from this source is the Vcm signal and the second is connected to a voltage source at 0.45-V. The positive terminal of the power supply is Vctrl and the negative terminal is ground, so from analyzes varying the width of the PMOS the most accurate value to obtain the expected output signal was 15.7 μm.

With the sized OTA, the operation verification is performed using the DDA. In this circuit, the width of the PMOS transistors in the DDA circuit was 14.0μm, thus obtaining the best operating performance so that the output signal achieves $\frac{VDD}{2}$. Transistors are operating in weak inversion region, thus large gate widths are necessary to provide the required transconductance gm. Transistors dimensions are summarized in Tab. I. The total gate area is 6,237 μm^2.

III. Simulation Results

The designed OTA was simulated at nominal temperature (27°C) and process corners using the Spectre circuit simulator. Fig. 3 depicts the open-loop OTA with a balanced capacitive load of 10 pF used in the testbench. The OTA is powered with a 0.9-V supply voltage. This OTA achieves a DC gain of 52.22 dB and provides a GBW of 36.66 MHz with a phase margin of 71.79º. Fig. 5 presents the frequency response of the designed OTA. The total current drained by this circuit is 226.34μA leading to a power consumption of 212.7μW. Tab. II summarizes the OTA performance.

The topology shown in Fig. 4 was used to simulate the OTA slew-rate, where both resistors have 1 MΩ resistance. It can be seen from Tab. II that for the positive ramp the value of 0.37 V/μs is obtained and for the negative ramp 0.36 V/μs, and the overall power consumption was 203.71 μW.

Tab. III presents the OTA main parameters across temperature variation. Although DC voltage gain and phase margin present small variation with temperature variation, GBW is highly affected.

The GBW variation is due to the fact that the increasing in temperature yields a decreasing in carrier mobility and threshold voltage. As the mobility decreases, the drain current

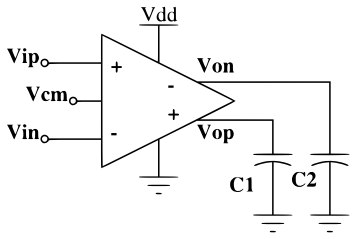

Fig. 3: OTA Design

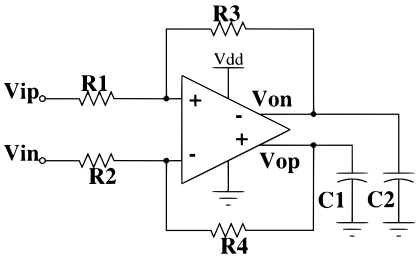

Fig. 4: Testbench to measure the OTA slew-rate.

decreases. At the same time, when the threshold voltage decreases, with low overdrive voltage, the drain current increases and, consequently, the transconductance increases. Thus, since GBW is proportional to the ratio of transconductance to load capacitance, it increases with increasing temperature [11].

A. Monte Carlo Simulation

Monte Carlo simulation computes the circuit performance when undergoing processing variations and transistor mismatch through random sampling. Thus, a 500-run Monte Carlo simulation was performed to evaluate the OTA main parameters. Figures 6 and 7 present the histogram of DC voltage gain and GBW considering process variations and mismatch.

The DC gain average and standard deviation are 52.15 dB and 91.76m dB, respectively. The GBW average and standard variation are 32.44 MHz and 4.75 MHz, respectively. Based on those results, it is possible to verify an stable DC gain while the GBW is highly dependent on process variations. Due to the wide GBW variation for both process and temperature, it is important to ensure a safety margin during the design phase to meet the project requirements.

TABLE II: Simulated performance for the designed Inverter-Based OTA.

Parameters	Value
Supply voltage (V)	0.90
Technology (nm)	180.00
DC voltage gain (dB)	52.22
Phase margin (°)	85.68
GBW (MHz)	36.66
Slew-Rate + (V/μs)	0.37
Slew-Rate - (V/μs)	0.36
Power consumption (μW)	203.71

TABLE III: OTA main performance parameters across temperature variation

	Temperature		
Parameter	-25°C	27°C	85°C
GBW (MHz)	20.37	36.66	54.18
PM (°C)	85.65	85.68	85.70
DC gain (dB)	52.49	52.22	51.59

Figure 8 presents the OTA differential output signal as a function of time. This wave can be used for the calculation of the slew-rate. The rise and fall time average slew-rate are close to 369 $\frac{V}{ms}$, as shown in Tab. IV.

To compare the performance of the designed OTA, a figures-of-merit (FOMs) was calculated according to the eq. 2.

This FOM serve in addition to determining the performance and speed of the OTA, where the higher the FOM, the faster the circuit and the lower the power consumption. Tab. IV summarizes the designed OTA performance and compares this work with other works present in the literature. It can be seen that the designed OTA obtained the second best performance with respect to other works for the FOM_S.

$$FOM_S = \frac{GBW \cdot C_L}{P_D} \left[\frac{MHz \cdot pF}{\mu W}\right] \quad (2)$$

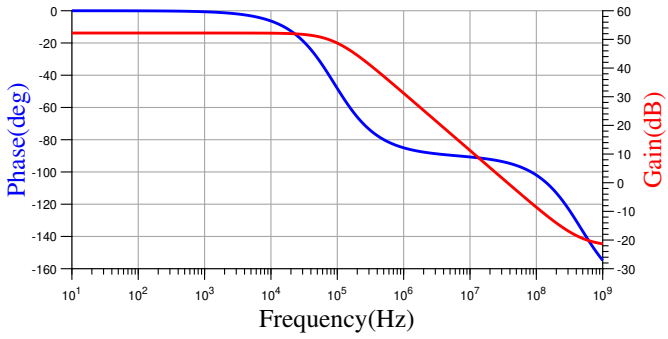

Fig. 5: Phase (blue) and voltage gain (red) simulation as a function of input frequency for nominal temperature and process parameters.

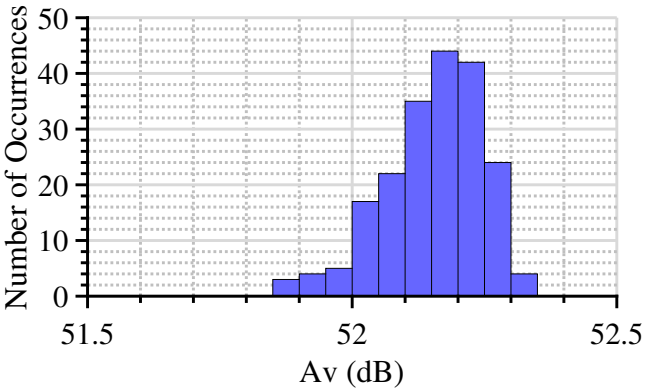

Fig. 6: Monte Carlo simulation of DC voltage gain.

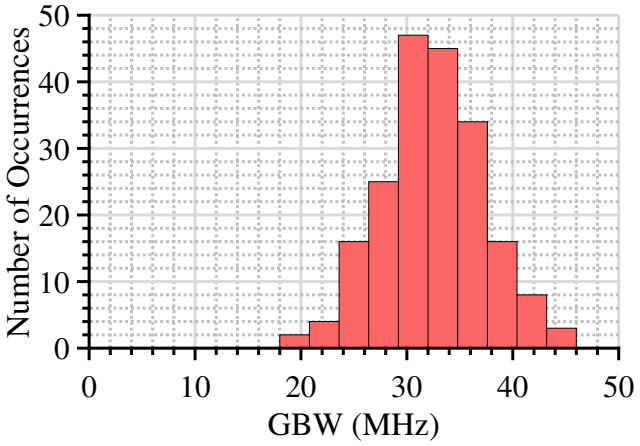

Fig. 7: Monte Carlo simulation of GBW.

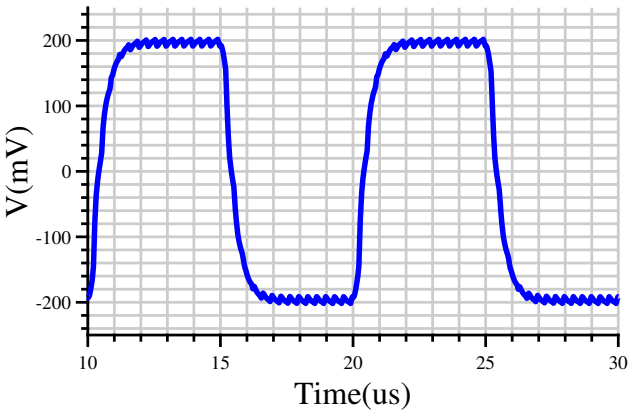

Fig. 8: Transient output voltage simulation for a square input signal.

IV. Conclusion

This work presented the results of design, characterization and simulation of a transconductance operational amplifier based on a self-biased inverter for sub-1 V applications in 180-nm CMOS technology. A CMFB circuit is used to control the common mode voltage at the outputs and attenuate the error signal. It was observed that with the control signal on the gate of the M5-M6 transistors, the circuit presented better stability in the 0.45-V point. As transistors operate in weak inversion, a good energy efficiency was obtained. The performance of the designed OTA is suitable for data converters and analog filters applications.

TABLE IV: Comparison table

	This Work	[9]*	[7]*	[6]	[5]
Year	2022	2018	2022	2020	2022
Tech node (μm)	0.18	0.18	0.18	0.18	0.13
VDD (V)	0.9	0.9	0.5	0.3	0.3
DC_{gain} (dB)	52.22	52.15	93.09	64.70	15.00
C_L (pF)	10	1	20	30	100
$GBW (MHz)$	36.666	37.180	0.018	0.002	0.006
PM (deg)	85.68	86.34	53.46	52	-
SR + (V/ms)	376.0	-	-	1.9	-
SR - (V/ms)	363.0	-	-	6.4	-
SR_{avg} (V/ms)	369.500	-	-	4.150	-
P_D (μW)	203.710	58.300	0.616	0.0126	0.708
FOM_S $\left(\frac{MHz.pF}{\mu W}\right)$	1.79	0.637	0.584	47.61	0.847
$Area$ (μm^2)	6,237[a]	-	932[a]	8,500[b]	965[b]

*OTA 1; *DDA; [a]gate area; [b]silicon area.

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